APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/713,776	11/13/2003	Alok Kumar	10559-878001 / P17397	8759

				EXAMINER
20985	7590	07/20/2006		SAVLA, ARPAN P

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ART UNIT	PAPER NUMBER
2185	

DATE MAILED: 07/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)
Office Action Summary	10/713,776	KUMAR, ALOK
	Examiner	Art Unit	
	Arpan P. Savla	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *26 April 2006*.

2a) ☐ This action is **FINAL**.   2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-37* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1-37* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☒ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a) ☐ All   b) ☐ Some * c) ☐ None of:

      1. ☐ Certified copies of the priority documents have been received.

      2. ☐ Certified copies of the priority documents have been received in Application No. _____.

      3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

This Office action is in response to Applicant's communication filed April 24, 2006 in response to the Office action dated January 24, 2005. Claims 11 and 24-29 have been amended. New claims 33-37 have been added. Claims 1-37 are pending in this application.

OBJECTIONS

Specification

1.　The title of the invention is still not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: "Allocating Content Addressable Memory (CAM) To A Microblock Of Instructions."

2.　In view of Applicant's amendment, the objections to the specification for failing to provide proper antecedent basis for the claimed subject matter have been withdrawn.

Claims

3.　In view of Applicant's amendment, the objections to **claim 26** have been withdrawn.

REJECTIONS NOT BASED ON PRIOR ART

Claim Rejections - 35 USC § 101

4.   In view of Applicant's amendment, the 101 rejections to **claims 11-20** have been

withdrawn.

Claim Rejections - 35 USC § 112

5.   The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly
> claiming the subject matter which the applicant regards as his invention.

6.   **Claim 37 is rejected under 35 U.S.C. 112, second paragraph, as being**

indefinite for failing to particularly point out and distinctly claim the subject

matter which applicant regards as the invention.

7.   **As per claim 37**, the claim recites the limitation "The networking device" in line 1.

There is insufficient antecedent basis for this limitation in the claim. Based on newly

new claims 33-36 the Examiner believes the claim was meant to read "The networking

device of claim of 27" in which case there would be sufficient antecedent basis for the

limitation in the claim. Therefore, for the purposes of examining the instant amendment

the Examiner will interpret the claim to read "The networking device of claim of 27."

8.   In view of Applicant's amendment, the 112 rejections to **claims 24-29** have been

withdrawn.

REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 103

9.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10.   **Claims 1-2, 4-5, 11-12, 14-15, 21-22, 24-25, 27-28, 30-31, and 33-37 are**

rejected under 35 U.S.C. 103(a) as being obvious over Pereira et al. (U.S. Patent

6,697,276) in view of Wolrich et al. (U.S. Patent Application Publication

2003/0115347).

11.   **As per claims 1 and 11**, Pereira discloses allocating a memory entry in a

memory device to instructions, a portion of the memory entry includes a unique identifier

assigned to the instructions (col. 18, lines 36-42 and 52-60). *It should be noted that*

computer program product in claims 11-20 executes the exact same functions as the

methods in claims 1-10. Therefore, any reference that teaches claims 1-10 also

teaches the corresponding claims 11-20. It should also be noted that it is inherently

required there be "instructions" associated with the "NFA operation" and therefore the

"CAM blocks... enabled to participate in the NFA operation" are analogous to "memory

entries allocated to instructions." Lastly, it should also be noted that the "entry type

value" is analogous to the "unique identifier."

Pereira does not expressly disclose a multithreaded engine included in a packet

processor.

Wolrich discloses a multithreaded engine included in a packet processor (paragraph 0014, lines 2-7; paragraph 0012, lines 1-4; Fig. 2, elements 18 and 21). *It should be noted that the "network processor" is analogous to the "packet processor,"*

Pereira and Wolrich are analogous art because they are from the same field of endeavor, that being content addressable memory (CAM).

At the time of the invention it would have been obvious to a person of ordinary skill in the art to use Wolrich's receive pipeline to process data packets within Pereira's CAM device.

The motivation for doing so would have been to not have the processor lie idle while waiting for all steps of the first instruction to be completed, therefore, pipelining can lead to improvements in system performance (Wolrich, paragraph 0014, lines 11-13).

Therefore, it would have been obvious to combine Pereira and Wolrich for the benefit of obtaining the invention as specified in claim 1.

12.   **As per claim 2 and 12**, the combination of Pereira/Wolrich discloses maintaining a count of threads that use the memory entry (Pereira, col. 56, lines 27-34).

13.   **As per claim 4 and 14**, the combination of Pereira/Wolrich discloses maintaining the count includes incrementing the count to represent a thread initiating use of the memory entry (Pereira, col. 56, lines 27-30). *It should be noted that when taking the broadest interpretation of the claim language it is clear that the limitations of the claim do not specify what determines "initiating use of the memory entry." Pereira discloses insertion of a CAM entry, thus, "initiating use of a CAM entry."*

14.   **As per claim 5 and 15**, the combination of Pereira/Wolrich discloses maintaining

the count includes decrementing the count to represent a thread halting use of the

memory entry (col. 56, lines 30-34). *It should be noted that when taking the broadest*

interpretation of the claim language it is clear that the limitations of the claim do not

specify what determines "halting use of the memory entry." Pereira discloses deletion

of a CAM entry, thus, "halting use of a CAM entry."

15.   **As per claim 21**, Pereira discloses a memory manager comprises:

a process to allocate a memory entry in a memory device to instructions, a

portion of the memory entry includes a unique identifier assigned to the instructions (col.

18, lines 36-42 and 52-60). *See the citation note for the similar limitation in claim 1*

above.

Pereira does not expressly disclose a multithreaded engine included in a packet

processor.

Wolrich discloses a multithreaded engine included in a packet processor

(Wolrich, paragraph 0014, lines 2-7; paragraph 0012, lines 1-4; Fig. 2, elements 18 and

21).

See the 103 rejections of claims 1 and 11 above for the reasons to combine

Pereira and Wolrich.

16.   **As per claim 22**, Pereira discloses a process to maintain a count of threads that

use the memory entry (col. 56, lines 27-34).

Wolrich discloses a multithreaded engine (paragraph 0014, lines 2-7; Fig. 2,

element 21).

17.   **As per claim 24**, Pereira discloses a system

to allocate a memory entry in a memory device to instructions, a portion of the

memory entry includes a unique identifier assigned to the instructions (col. 18, lines 36-

42 and 52-60). *See the citation note for the similar limitation in claim 1 above.*

Pereira does not expressly disclose a multithreaded engine included in a packet

processor.

Wolrich discloses a multithreaded engine included in a packet processor

(Wolrich, paragraph 0014, lines 2-7; paragraph 0012, lines 1-4; Fig. 2, elements 18 and

21).

See the 103 rejections of claims 1 and 11 above for the reasons to combine

Pereira and Wolrich.

18.   **As per claim 25**, Pereira discloses a system configured to maintain a count of

threads that use the memory entry (col. 56, lines 27-34).

Wolrich discloses a multithreaded engine (paragraph 0014, lines 2-7; Fig. 2,

element 21).

19.   **As per claim 27**, Pereira discloses a network forwarding device

to allocate a memory entry in a memory device to instructions, a portion of the

memory entry includes a unique identifier assigned to the instructions (col. 18, lines 36-

42 and 52-60). *See the citation note for the similar limitation in claim 1 above.*

Pereira does not expressly disclose a network forwarding device comprising:

an input port for receiving packets;

an output for delivering the received packets;

a network processor;

and a multithreaded engine included in a packet processor.

Wolrich discloses a network forwarding device comprising:

an input port for receiving packets (paragraph 0011, lines 1-3; Fig.1, element 12);

an output for delivering the received packets (paragraph 0011, lines 3-5; Fig. 1, element 16);

a network processor (paragraph 0011, lines 5-8; Fig 1, element 18);

and a multithreaded engine included in a packet processor (Wolrich, paragraph 0014, lines 2-7; paragraph 0012, lines 1-4; Fig. 2, elements 18 and 21).

See the 103 rejections of claims 1 and 11 above for the reasons to combine Pereira and Wolrich.

20.   **As per claim 28**, Pereira discloses a network forwarding device configured to maintain a count of threads that use the memory entry (col. 56, lines 27-34).

Wolrich discloses a multithreaded engine (paragraph 0014, lines 2-7; Fig. 2, element 21).

21.   **As per claim 30**, Pereira discloses a method comprising:

allocating a content-addressable-memory (CAM) entry to a microblock, a portion of the CAM entry includes a unique identifier assigned to the microblock (col. 18, lines 36-42 and 52-60). *It should be noted that the "instructions" of the "NFA operation" are analogous to the "microblock."*

Pereira does not expressly disclose a multithreaded microengine included in a network processor.

Wolrich discloses a multithreaded microengine included in a network processor

(paragraph 0014, lines 2-7; paragraph 0012, lines 1-4; Fig. 2, elements 18 and 21).

See the 103 rejections of claims 1 and 11 above for the reasons to combine

Pereira and Wolrich.

22.   **As per claim 31**, Pereira discloses maintaining a count of threads that use the

CAM entry (col. 56, lines 27-34).

Wolrich discloses a multithreaded microengine (paragraph 0014, lines 2-7; Fig. 2,

element 21).

23.   **As per claims 33-37**, Pereira discloses the memory entry comprises a content-

addressable memory entry (col. 18, lines 36-37).

24.   **Claims 3, 6-10, 13, 16-20, 23, 26, 29, and 32 are rejected under 35**

U.S.C. 103(a) as being obvious over Pereira in view of Wolrich as applied to

claims 1, 21, 24, 27, and 30 above, and further in view of Litt et al. (U.S Patent

Application Publication 2003/0126358).

25.   **As per claims 3 and 13**, the combination of Pereira/Wolrich discloses all the

limitations of claim 3 except maintaining a bit to represent availability of the memory

entry for thread use.

Litt discloses maintaining a bit to represent availability of the memory entry for

thread use (paragraph 0035, lines 7-9; Fig. 1, element 170). *It should be noted that the*

"output of the AND gate" is either a high or low voltage. A bit is represented physically

by either a high or low voltage. Therefore, the "output of the AND gate" is analogous to

a "bit."

The combination of Pereira/Wolrich and Litt are analogous art because they are from the same field of endeavor, that being content addressable memory (CAM).

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Litt's valid bit within Pereira/Wolrich's CAM block.

The motivation for doing so would have been to have a technique which permits software loops to be detected and eliminates multiple iterations of a software loop from being stored in memory as part of a PC trace, thus, reducing memory consumption (Litt, paragraph 0018, lines 1-4).

Therefore, it would have been obvious to combine Pereira, Wolrich, and Litt for the benefit of obtaining the invention as specified in claims 3 and 13.

26.   **As per claims 6 and 16**, the combination of Pereira/Wolrich/Litt discloses maintaining the bit includes setting the bit to represent availability of the memory entry for thread use (Litt, paragraph 0036, lines 25-32).

27.   **As per claims 7 and 17**, the combination of Pereira/Wolrich/Litt discloses maintaining the bit includes clearing the bit to represent unavailability of the memory entry for thread use (Litt, paragraph 0036, lines 32-38).

28.   **As per claims 8 and 18**, the combination of Pereira/Wolrich/Litt discloses checking the bit to determine the availability of the memory entry for thread use (Litt, paragraph 0035, lines 7-9).

29.   **As per claims 9 and 19**, the combination of Pereira/Wolrich/Litt discloses the unique identifier includes four bits (Lit, paragraph 0037, lines 4-5; paragraph 0038, lines 26-27). *It should be noted that "Mask signal" is analogous to "unique identifier."*

30.   **As per claims 10 and 20**, the combination of Pereira/Wolrich discloses a

multithreaded engine of the packet processor (Wolrich, paragraph 0014, lines 2-7;

paragraph 0012, lines 1-4; Fig. 2, elements 18 and 21).

Litt discloses the memory entry identifies a location in a local memory (paragraph

0019, lines 4-8). *It should be noted that "instruction address" is analogous to "identifier*

of a location in a local memory."

31.   **As per claim 23**, the combination of Pereira/Wolrich/Litt discloses a process to

maintain a bit to represent availability of the memory entry for thread use (Litt,

paragraph 0035, lines 7-9; Fig. 1, element 170).

32.   **As per claim 26**, the combination of Pereira/Wolrich discloses a packet

processor (Wolrich, paragraph 0012, lines 1-4; Fig. 2, element 18).

Litt discloses maintaining a bit to represent availability of the memory entry for

thread use (paragraph 0035, lines 7-9; Fig. 1, element 170).

33.   **As per claim 29**, the combination of Pereira/Wolrich discloses a network

processor (Wolrich, paragraph 0012, lines 1-4; Fig. 2, element 18).

Litt discloses maintaining a bit to represent availability of the memory entry for

thread use (paragraph 0035, lines 7-9; Fig. 1, element 170).

34.   **As per claim 32**, the combination of Pereira/Wolrich/Litt discloses maintaining a

bit in a status register to represent availability of the CAM entry to identify a local

memory location (Litt, paragraph 0038, lines 3-5; Fig. 2, element 250).

Response to Arguments

35.   Applicant's arguments, see page 10, lines 2-4, of the communication filed April 24, 2006, with respect to the rejections of **claims 1-32** under 35 USC § 103 have been fully considered and are persuasive. Therefore, the rejections have been withdrawn. However, upon further consideration, new grounds of rejection have been made under 35 USC § 103 with respect to **claims 1-37** as presented above.

Conclusion

STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by MPEP 707.70(i):

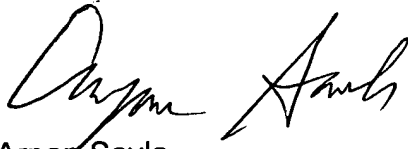### CLAIMS REJECTED IN THE APPLICATION

Per the instant office action, **claims 1-37** have received a second action on the merits and are subject of a second action non-final.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Arpan P. Savla whose telephone number is (571) 272-1077. The examiner can normally be reached on M-F 8:30-5:00.
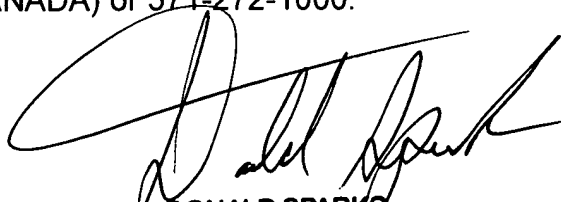
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the

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Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a

USPTO Customer Service Representative or access to the automated information

system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Arpan Savla
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Art Unit 2185
July 13, 2006

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